

PATENT APPLICATION

042390.P11991

Amendment**Amendment to Specification**

Please amend the paragraph starting on page 3, line 16 as shown:

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, together with objects, features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

Figure 1 is a block diagram of an integrated circuit according to an embodiment of the present invention;

Figure 2 is a clamp circuit having a stacked-gate PMOS transistor;

Figure 3 is a clamp circuit having a stacked-gate PMOS transistor;

Figure 4 is an alternate embodiment of the present invention; [and]

Figure 5 is an alternate ESD circuit in accordance with an alternate embodiment of the present invention [.] ; and

Figure 6 is a clamp circuit having three tiers in accordance with another embodiment of the present invention.

Please amend the paragraph starting on Page 7, line 3 as shown:

Although the scope of the present invention is not limited in this respect, ESD protection circuit 104 may comprise two or more tiers, such as the two tiers 120 and 130 as shown in FIG. 2. The tiers 120 and 130 may include one of the transistors of current sinking circuit 202, one of gate drive circuits 212 and 214, and one of transistors of voltage divider circuit 216. In other words, tiers 120 and 130 may represent the logic associated with one or more transistors in a current sinking circuit or with one or more transistors in a voltage divider circuit in the ESD

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protection circuit. It should also be understood that although only two tiers are shown in FIG. 2, alternative embodiments of the present invention may have three or more tiers as desired. For example, FIG. 6 illustrates an embodiment having a third tier 630 and a current sinking transistor 606.

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Please amend the Abstract as shown below.

Abstract

**[Briefly, in accordance with one embodiment of the invention, an] An
electrostatic discharge circuit may include an RC timer that may be used to control
the operation of two or more tiers within the ESD circuit.**